Fast-Switching Routing Logic for High-Speed Interleaving Operation of a Multichannel Time-to-Amplitude Converter

Mehmet Ali Uluisik, Jacopo Campora, Mehmet Caglar Koca, Giulia Acconcia & Ivan Rech

Politecnico di Milano, Piazza Leonardo da Vinci 32, 20133, Milan, Italy

Fluorescence imaging plays a fundamental role in modern scientific research, enabling the non-invasive observation of molecular dynamics through the detection of weak and fast optical signals. Among the available techniques, Time-Correlated Single Photon Counting (TCSPC) is widely considered the gold standard for measuring such ultra-fast, low-intensity events, providing temporal resolutions on the order of picoseconds. However, conventional TCSPC systems suffer from the pile-up effect at high photon count rates. To minimize this distortion, the average detected photon rate must typically be kept below approximately 0.05 photons per excitation period. This constraint significantly reduces measurement efficiency and ultimately prevents the realization of true real-time fluorescence imaging. A recent TCSPC method [1] exploits monitoring system activity to completely overcome this limitation. Using this method, ultrafast Silicon Photomultipliers (SiPMs) with sub-nanosecond dead times can be effectively employed to acquire multiple photons per excitation period. Despite this advancement, a new bottleneck arises: the intrinsic dead time of the backend timing circuits. Although state-of-the-art timing circuits provide high precision and linearity, their limited conversion rates restrict the overall system throughput. To break this speed barrier, we propose a multichannel interleaved architecture that utilizes eight single-channel Time-to-Amplitude Converters (TACs) via a specialized routing chip (Fig. 1a). The parallelized TAC array integrates eight independent TACs on the same silicon die, derived from a validated single-channel design [2]. The converter was designed in 350 nm SiGe technology to benefit from its high-speed bipolar transistors, achieving a 1.9 ps rms precision and high linearity, though at the expense of a limited 10 Mcps conversion rate. The routing logic performs the interleaving function; through its 1-to-8 structure, it consecutively redirects incoming pulses from the detector to the parallel TAC array, effectively enabling high-count-rate, multi-photon processing without sacrificing timing precision. The post-layout simulations of the routing logic designed in 55 nm technology confirm a high input rate of 1.67 Gbps (Fig. 1b) with a negligible added jitter of 0.46 ps rms. This work demonstrates that combining heterogeneous semiconductor technologies enables a high-throughput timing system capable of fully exploiting next-generation single-photon detectors.

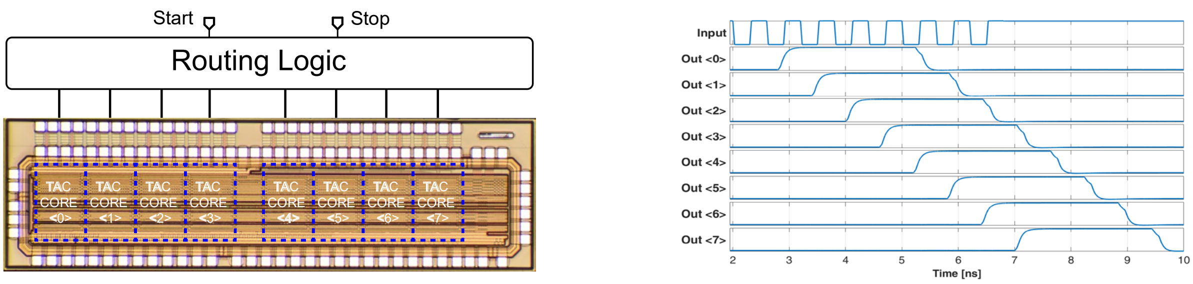

Fig. 1: *(a) Schematic diagram of the proposed system with the die photograph of the 8-parallel TAC. (b) Output waveforms of the routing logic at the maximum input rate with 300 ps spacing.*

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References

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