

SPAD array with signal and idler TDCs for asynchronous Quantum Ghost Imaging

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Quantum Ghost Imaging (QGI) enables spectral separation between interacting photons (idler) and detected photons (signal). In typical QGI setups, infrared idler photons interacting with the target are collected by a single-pixel bucket detector, while entangled visible signal photons are detected by a camera. While early implementations relied on optical delay lines to compensate path-length differences [1], more recent asynchronous approaches (aQGI) [2], based on photon time-stamping and coincidence correlation, showed that more flexible and scalable architectures are feasible.

This work presents the design of a camera based on a new chip designed for aQGI integrating both a 64×64 Single-Photon Avalanche Diode (SPAD) array with in-pixel shared time-to-digital converters (TDCs) for signal photon time-tagging and a high resolution single-hit TDC for idler events from an external bucket detector (e.g., an InGaAs/InP SPAD). The chip is integrated in a custom two-board stacked system, controlled by a FPGA board that generates control signals, reads the chip outputs, and manages communication with the custom camera software on the computer.

The camera maximizes measurement efficiency by improving Photon Detection Efficiency (PDE), duty cycle, and frame rate. The overall PDE (55 % @ 550 nm) is achieved thanks to the choice of an advanced 3D-stacked technology: the SPADs are fabricated in the dedicated top tier, vertically integrated onto a CMOS 40 nm logic bottom tier. This architecture enables a high fill-factor, further increased by integrated microlenses. Due to the dense layout, the array is divided into 1024 macro-pixels, each sharing a counter-based TDC (300 ps LSB, 1.2 ns FSR) driven by an on-chip PLL, together with local control and readout logic. In order to achieve a high duty cycle, the camera implements a pipeline architecture that parallelizes photon acquisition and readout, thus greatly reducing the percentage of blind time in each frame. Frame rate is further increased through an event-driven skip-readout scheme, which, combined with the low photon flux typical of QGI, enables operation up to 1 MHz with near-unity duty cycle. Compared with previous QGI signal cameras, idler time-tagging is performed on-chip by a stand-alone TDC (75 ps LSB, 1.2 ns FSR), simplifying synchronization between signal and idler events.

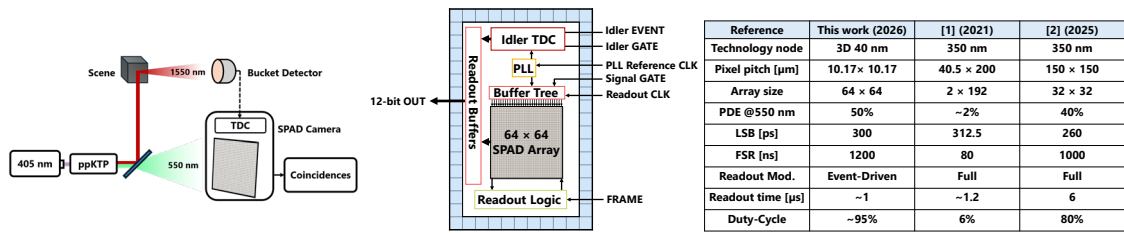


Fig. 1: (a) aQGI setup with the proposed SPAD camera, (b) Block diagram of the SPAD chip, (c) Comparison table.

This project has received funding from the European Defence Fund (EDF) under grant agreement EDF-2021-DIS-RDIS-ADEQUADE. Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or the European Commission. Neither the European Union nor the granting authority can be held responsible for them.

References

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